

Silicon Profile Transformation and Sidewall Roughness Reduction Using Hydrogen Annealing

Ming-Chang M. Lee, Jin Yao and Ming C. Wu

Department of Electrical Engineering, University of California at Los Angeles
Los Angeles, CA 90095-1594

ABSTRACT

We report on a comprehensive study of the 3-D profile transformation process for microstructures on silicon-on-insulator (SOI) substrates. Using hydrogen annealing, single crystalline microspheres (1 μm radius), micropillars, and circular cantilever beams have been successfully demonstrated. The annealed Si exhibits a surface roughness of 0.26 nm. A theoretical model is presented for the mass transport process, and the parametric dependence on temperature and pressure is characterized. We have used this process to fabricate sub-micrometer single mode optical waveguides on SOI and achieved a very low optical loss of 0.2 cm^{-1} .

1. INTRODUCTION

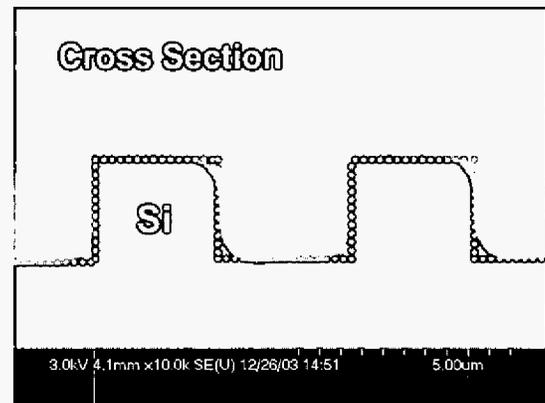
Three-dimensional (3-D) microstructures with rounded profiles and smooth sidewalls have many interesting applications. Previously, most of such structures were made by reflow technique. However, they are limited to noncrystalline materials such as glasses [1] or polymers [2]. Recently, thermal annealing in hydrogen ambient has been demonstrated to produce rounded profiles [3][4] and remove surface roughness on bulk silicon [5][6]. It is believed that the heated hydrogen facilitates the migration of Si atoms [7] at temperatures much lower than the melting point (1414°C). Though this process has been extensively used in semiconductor manufacturing, most of the previous studies were performed on bulk Si. Recently, we found hydrogen annealing can transform etched silicon-on-insulator (SOI) islands into convex 3-D structures such as microspheres and circular beams [8]. In contrast to the reflow technique, the crystalline structures are preserved in this mass transport process.

In this paper, we present comprehensive experimental and theoretical investigations of this 3-D transformation process. We also demonstrate the use of hydrogen annealing to smooth the scalloping sidewalls created by deep reactive ion etching (DRIE) process. Potential applications in ultra-low-loss nanophotonic waveguides on SOI are described.

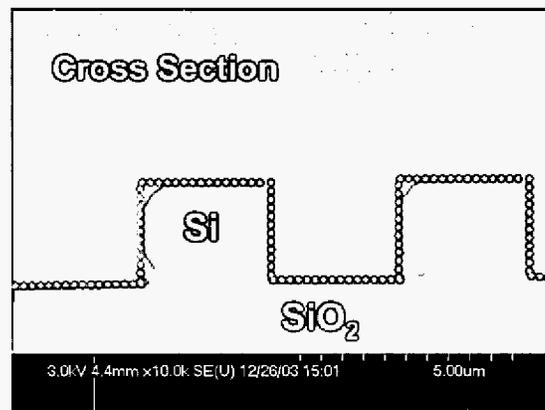
2. PROFILE TRANSFORMATION

Mechanism

Due to the enhanced surface mobility, Si atoms will migrate to smooth sharp edges and corners to minimize the surface energy. The resulting shapes are very different for bulk Si and SOI structures. Figure 1 compares the cross-sectional scanning electron micrographs (SEM) of the annealed rectangular features on bulk silicon and SOI. Both samples were annealed in pure hydrogen at 1100°C, 10 Torr for 5 minutes. Before annealing, the SOI wafer was etched to expose the buried oxide. The hydrogen-induced etching at Si-SiO₂ interface [9] produces all-convex corners. This enables us to make circular features, such as microspheres and micropillars (Figure 2).



(a)



(b)

Figure 1. Cross-sectional SEM images of the annealed profiles on (a) bulk Si and (b) SOI (1100°C, 10Torr, 5

minutes). The dash lines indicate the original profiles before annealing.

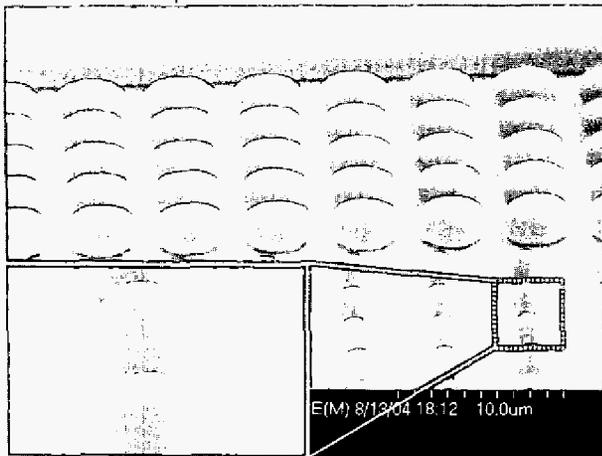


Figure 2. SEM images of microspheres and micropillars. The inset shows the magnified image on microspheres. The radius of each microsphere is about 1 μm.

If the sample is annealed for a long time, the SOI structure could completely separate from the buried oxide, resulting in self-released circular cantilever beams. This is illustrated in Figure 3, together with the SEM micrograph of the circular cantilever beams.

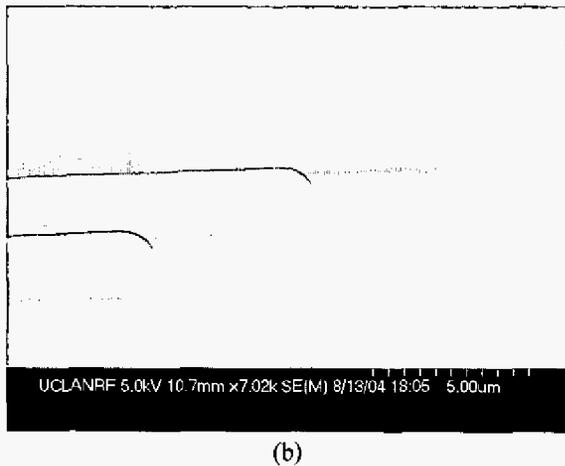
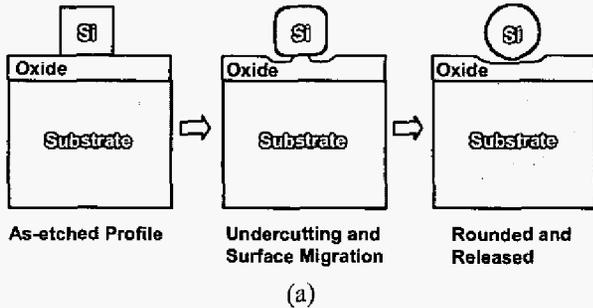


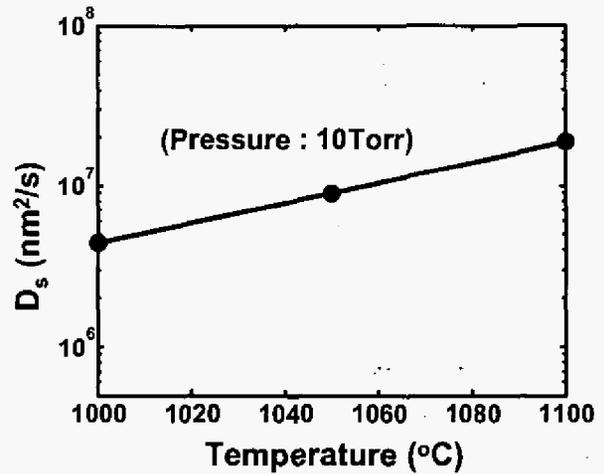
Figure 3. (a) Schematic process flow and (b) SEM image of circular cantilever beams. The diameter of each beam is about 2 μm.

Influence of Processing Parameters

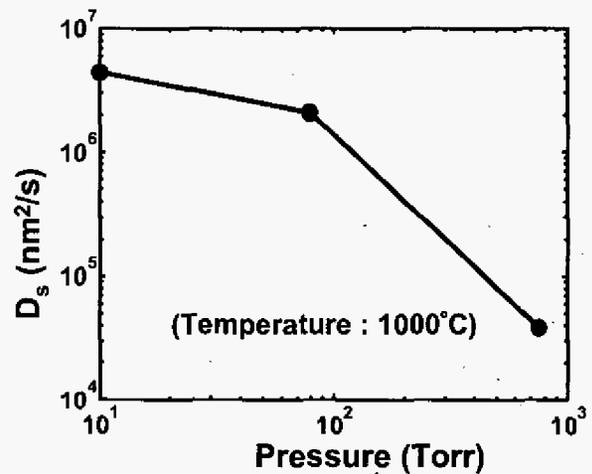
The shapes of the annealed structures depend on several parameters, including temperature, pressure, and time as well as the dimensions of the initial structures. To gain more insight, we have investigated the theoretical model for the process. The surface-enhanced mass transport can be described by Mullins' model [10]:

$$v_n = C_s \cdot \frac{D_s}{kT} \cdot \frac{\partial^2 K}{\partial s^2} \quad (1)$$

where v_n is the speed of the surface atoms moving along the normal direction, C_s is a material constant, D_s is the surface diffusion coefficient, K is surface curvature, and s is arc length along the profile. Among these parameters, D_s is strongly dependent on temperature and pressure. Based on this model, we have performed a parametric study of the corner evolution experimentally, and extracted the surface diffusion coefficients at various pressures and temperatures. As shown in Figure 4, the diffusion coefficient increases steadily with temperature, and reduces with pressure. The reduction becomes more dramatic when it is close to atmospheric pressure.



(a)



(b)

Figure 4. Surface diffusion coefficient as a function of (a) temperature and (b) pressure.

The diffusion of Si atoms along the surface is also driven by the local curvature. To explore this characteristic, we analyzed the corner evolution on a right-angle profile on a silicon step. Figure 5 shows the radius of curvature of a rounded corner versus annealing time at 1000°C, 1050°C, and 1100°C. As shown from these curves, the radius of curvature initially increases very rapidly, but after a few minutes, the increase becomes much slower. The radius of curvature approximately increases with the 4th root of time. The result also shows the radius is larger as the annealing temperature increases.

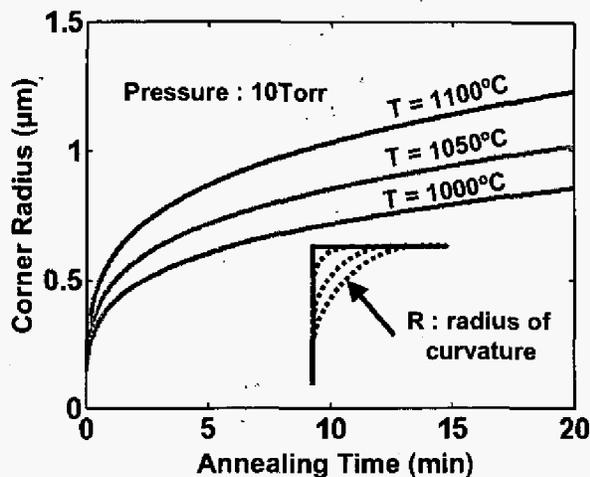


Figure 5. The evolution of the radius of curvature on the top corner of a mesa structure at 1000°C, 1050°C, and 1100°C.

3. SIDEWALL ROUGHNESS REDUCTION

Smoothing of Sidewall Scalloping

The theoretical model provides important guidelines for optimizing the process for different applications. If the dimensions of the SOI structure are smaller than the radius of curvature, the structure will be completely rounded (such as the microspheres in Figure 2). On the other hand, if the dimensions are much larger than the radius of curvature, the local roughness is smoothed out while the global shape remains largely unchanged. The latter process is useful for reducing sidewall roughness, which is important for various applications, including vertical micromirrors and microfluidic channels.

DRIE has been extensively used in bulk micromachining to create high-aspect-ratio structures. However, sidewall scalloping is usually formed due to the cyclic etching and deposition steps. Sacrificial thermal oxidation has been employed to improve sidewall quality; however, the process consumes too much material and easily builds up residual stress. Here, we demonstrate the

ability of hydrogen annealing to reduce sidewall roughness. Figure 6(a) shows the SEM of an as-etched mesa with rough sidewall scalloping after DRIE. The root-mean-square surface roughness is estimated to be 100 nm. After the wafer was annealed in pure hydrogen at 1100°C, 10Torr for 10 minutes, the surface roughness on both the sidewall and the substrate was dramatically reduced (Figure 6(b)). The width of structure remained the same.

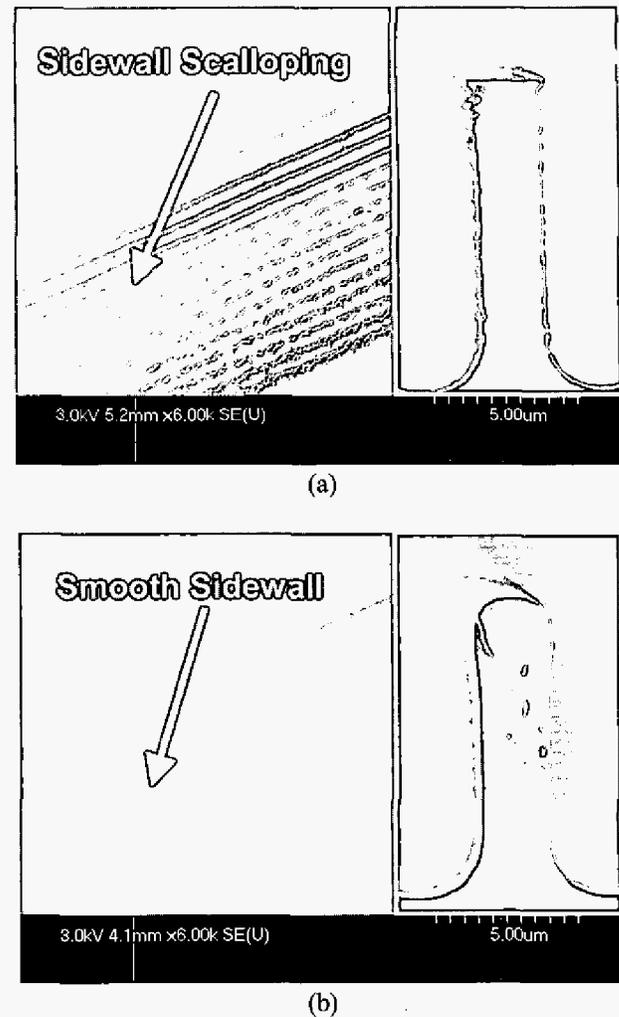


Figure 6. The sidewall roughness on a 10μm high, 2.5μm wide mesa (a) before annealing and (b) after annealing. The insets show the cross sections.

Measurement of Sidewall Roughness

To obtain quantitative measurement on sidewall roughness reduction, an atomic force microscope (AFM) was used to study surface morphology. A shallow step was first etched by conventional dry etching technique. After the sample was annealed at 1100°C, 10Torr for 10 minutes, the vertical sidewall became sloped. It facilitates the AFM tip to scan across the sidewall surface. Figure 7 displays the image of a 200nm×200nm scanning area on the sidewall. The data shows that the root-mean-square roughness of the annealed surface is only 0.26 nm.

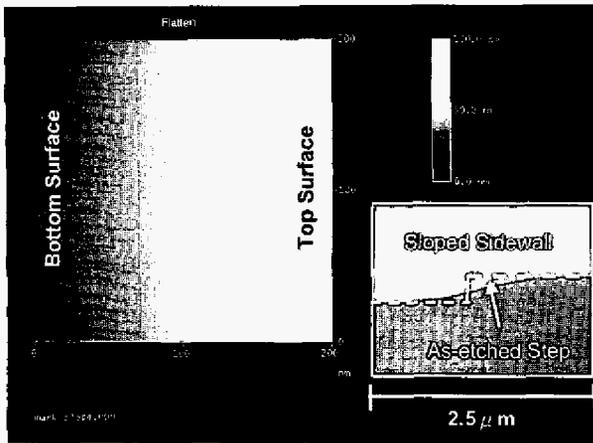


Figure 7. Atomic force microscope images of the silicon sidewall surface after hydrogen annealing. The scan area is 200nm by 200nm. The measured data shows the rms roughness is 0.26nm

Applications

One application of this novel process is very low loss single-mode optical waveguide on SOI. Sub-micron waveguides are needed to achieve single mode operation due to the large index contrast between Si and air. Such small waveguide are prone to scattering loss. Sub-nm surface roughness is required to achieve optical loss less than 1 dB/cm. Using the hydrogen annealing process, we have made a low loss optical wire with 0.5 μm width and 0.2 μm thickness (Figure 8), and achieved an optical loss of 0.2 cm^{-1} .

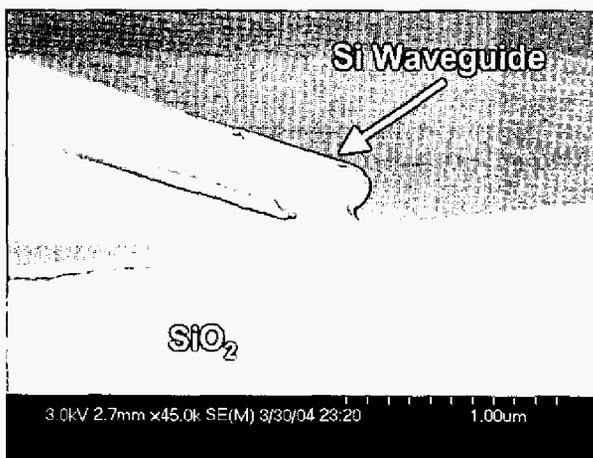


Figure 8. SEM image of a low-loss single-mode optical waveguide on SOI.

4. CONCLUSION

In summary, we have presented a comprehensive study of the hydrogen annealing process for SOI structures. Both profile transformation and sidewall roughness reduction are reported. We have achieved a sidewall roughness of 0.26

nm, and demonstrated an ultra-smooth submicron optical waveguide on SOI with an optical loss of 0.2 cm^{-1} . The processes for making microspheres, micropillars, and circular cantilever beams are also presented.

5. ACKNOWLEDGEMENT

This project is supported by DARPA/CS-WDM programs (#MDA972-02-1-0019).

6. REFERENCES

- [1] P. Jeuch, J. P. Joly, and J. M. Hode, "P-glass reflow with a tunable CO₂ laser", Laser and Electron Beam Interactions with Solids. Proceedings of the Materials Research Society Annual Meeting. North-Holland. Amsterdam, Netherlands, pp.603~608, 1982
- [2] H. Yang, C. -K. Chao, C. -P. Lin, and S. -C. Shen, "Micro-ball lens array modeling and fabrication using thermal reflow in two polymer layers", *J. of Micromech. Microeng.*, 14, pp. 277~282, 2004
- [3] Tsutomu Sato, Nobutoshi Aoki, Ichiro Mizushima, and Yoshitaka Tsunashima, "A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) Induced by Silicon Surface Migration", *IEDM 1999*, pp. 517~520
- [4] Hitoshi Kuribayashi, Reiko Hiruta, Ryosuke Shimizu, Koichi Sudoh, and Hiroshi Iwasaki, "Shape Transformation of Silicon Trenches during Hydrogen Annealing", *J. Vac. Sci. Technol. A* 21(4), pp 1279-1283, Jul/Aug. 2003
- [5] Nobuhiko Sato and Takao Yonehara, "Hydrogen Annealed Silicon-on-insulator", *Applied Physics Letter*, Vol. 65, No. 15, pp.1924~1926, Oct. 1994
- [6] Yang-Kyu Choi, Leland Chang, Pushkar Ranade, Jeong-Soo Lee, Daewon Ha, Sriram Balasubramanian, Aditya Agarwal, Mike Ameen, Tsu-Jae King, and Jeffery Boker, "FinFET Process Refinements of Improved Mobility and Gate Work Function Engineering", *International Electron Devices Meeting. Technical Digest*, pp259~262, 2002
- [7] S. Jeong and A. Oshiyama, "Complex diffusion mechanisms of a silicon adatom on hydrogenated Si (001) surface: on terraces and near steps", *Surface Science*, 433-435, pp. 481~485, 1999
- [8] M. -C. Lee and Ming C. Wu, "3D Silicon Transformation using Hydrogen Annealing", *Solid-State Sensor, Actuator, Microsystems Workshop*, Hilton Head, USA, pp. 19~22, 2004
- [9] S. T. Liu, L. Chan, and J. O. Borland, "Reaction Kinetics of SiO₂/Si(100) Interface in H₂ Ambient in A Reduced Pressure Epitaxial Reactor", *Proc. Electrochem. Soc.*, 87-88, pp428~434, 1987
- [10] W. W. Mullins, "Theory of Thermal Grooving", *Journal of Applied Physics*, Vol.28, No. 3, pp. 333~33, 1957